Preliminary Application Note

TDA1564/5

AN10304_1

Philips Semiconductors

TRAD

TPAN02_02W97

Revision history

Version Number	Date	Remarks	Author
0.1	04-05-02	Preliminary	Sebastien Kasman

Application Note

TDA1564/5

AN10304_1

Sebastien Kasman

Philips Semiconductors
Innovation Centre Nijmegen
The Netherlands

Keywords

Stereo power amplfier
high efficiency
cool power
SE / BTL

Number of pages : 29

Date: 2004-05-02

Summary

This Application note describes the stereo power amplifier TDA1564 and TDA1565 , primarily used in Car radio applications. With its' special amplifier topology, Cool Power, it has a higher efficiency than the standard class A/B amplifier type.

Contents

1. INTRODUCTION

1.1 Amplifier Description

The TDA1564 and TDA1565 amplifier are both high efficiency amplifiers with only some small differences. The differences can be found in the following table.

	TDA1564	TDA1565
Connected Load	2 x 4 Ohm	2 x 2 Ohm
Typical Output Power 10%thd @ specified load	2 x 25 Watt	2 x 40 Watt
Package	HSOP20 DBS17P	HSOP20
Diagnostics	Clip-, thermal-shortcircuit-**offset**-detection	Clip-, thermal-shortcircuit-detection

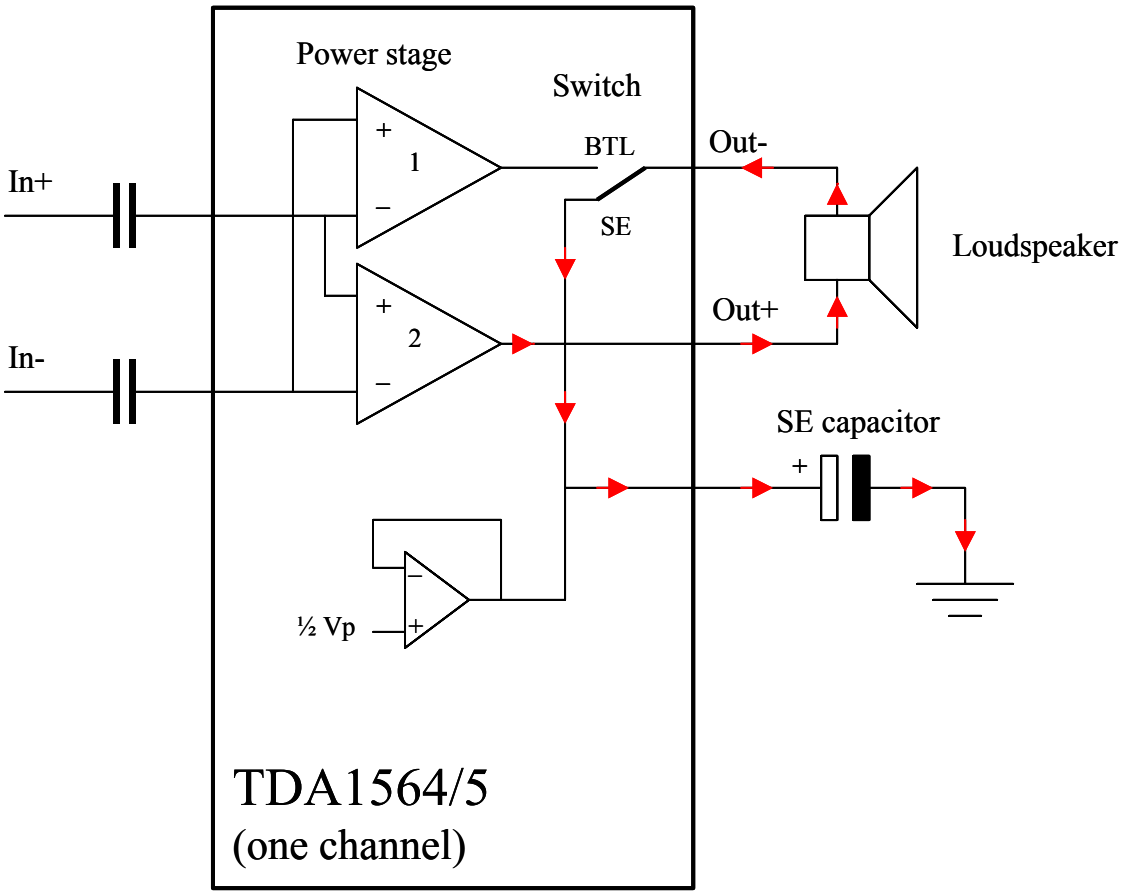
Comparison Table

The TDA1564/5 contains two identical amplifiers with differential inputs. At low output power, up to output amplitudes of approximately 2.5Vrms at Vp=14.4V and a 4 Ohm load , the device operates as a normal Single Ended (SE) amplifier. When a larger output voltage swing is needed, the circuit switches internally to Bridge Tied Load (BTL) operation. In this way the BTL function is only enabled during higher output powers. During lower output powers in SE mode, the amplifier is highly efficient because then it uses an external single-ended capacitor to create a non-dissipating half supply voltage.

The switch over voltage level from SE to BTL depends on the value of Vp. When Vp is decreasing, the switch over voltage level decreases also and vice versa, due to the switch over circuit design. eg. at higher Vp levels the master amplifier has more 'room' in SE mode for driving the load until switch over to BTL is necessary, the opposite is valid for lower Vp values, where the master has less driving 'room'. The following paragraphs explain the master/slave amplifier.

1.1.1 Single Ended mode

During SE mode the following (simplified) block diagram shows the current flow, when the switch(*) is in SE mode.



As can be seen in the drawing above, when the output voltage is lower than 2.5Vrms the SE switch remains closed. The current flows (during the positive half of the sinewave) from amplifier stage 2 (master) through the load, via the SE capacitor to ground.

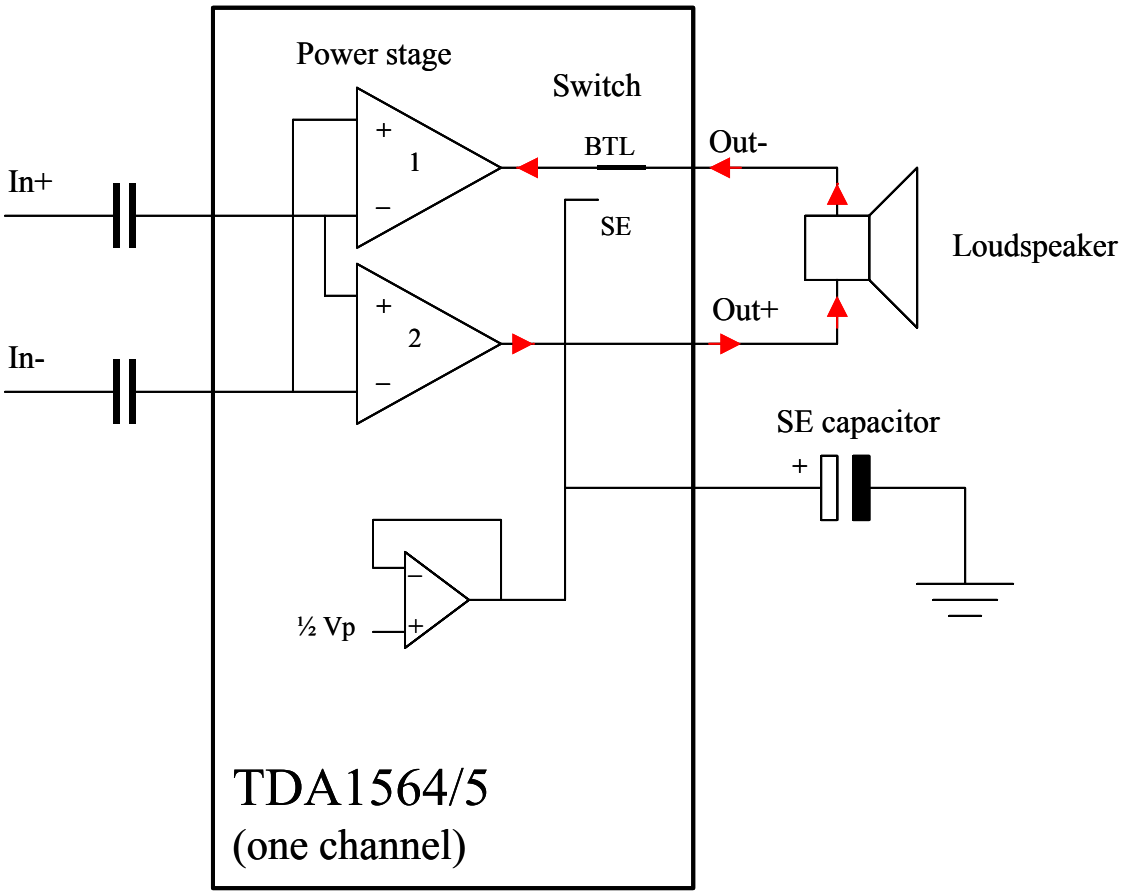
The small circuit at the bottom is a voltage buffer which keeps the voltage of the SE capacitor at ½ Vp.

The gain is internally controlled to 26dB by the master, stage 2.

(* The electronic mechanism that switches between SE and BTL is not a real switch but a complex circuit which has a gradual transition between SE and BTL)

1.1.2 Bridge Tied load

During BTL mode the following (simplified) block diagram shows the current flow, when the switch is in BTL mode.



As can be seen in the drawing above, when the output voltage is higher than 2.5Vrms, the BTL switch is closed. Now, the slave amplifier is enabled and current flows (during the positive half of the sinewave) from the master output through the load, to the slave.

Now, the output voltage of the slave (power stage 1) is of opposite phase with the output voltage of the master (power stage 2).

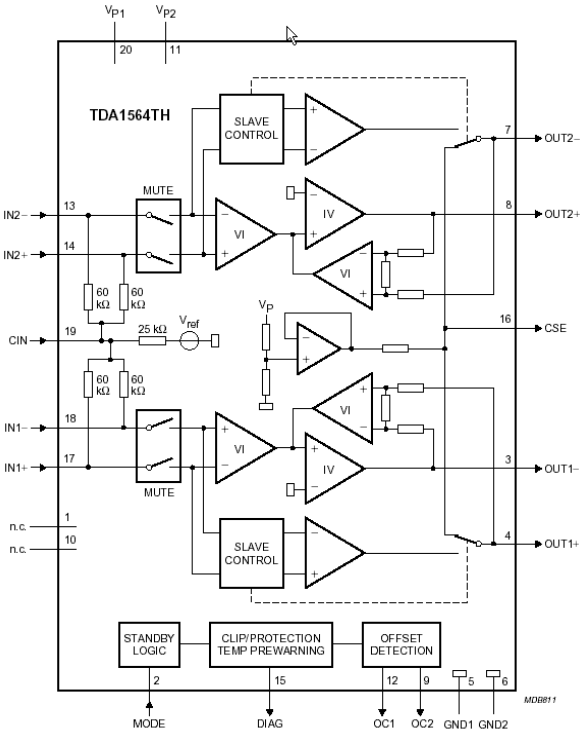
While the TDA1564/5 works in BTL, the total gain (of both amplifiers working together) remains 26dB.

When the junction temperature exceeds 150 C° the internal thermal protection will disable the BTL mode and the output power decreases to 5W in 4 Ohm for the TDA1564 and to 10W in 2 Ohm for the TDA1565.

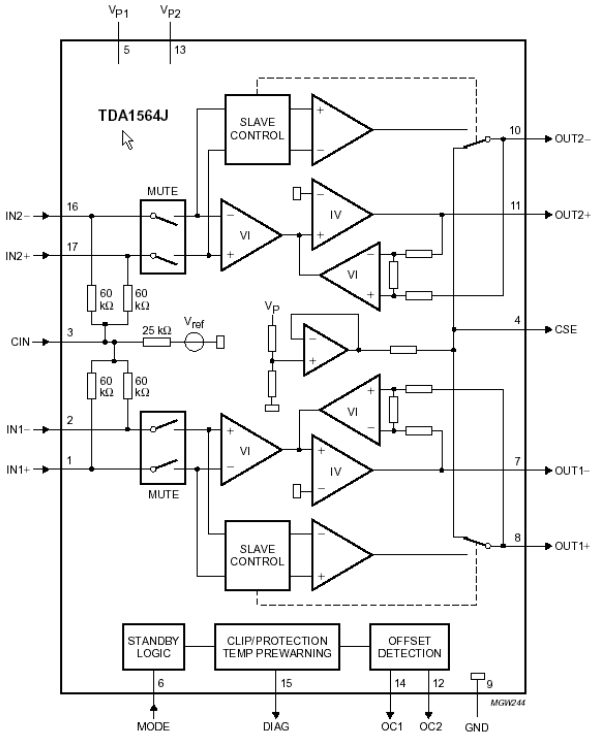
More details about the functional description can be found in the specification of the TDA1564/5.

1.2 Block Diagram

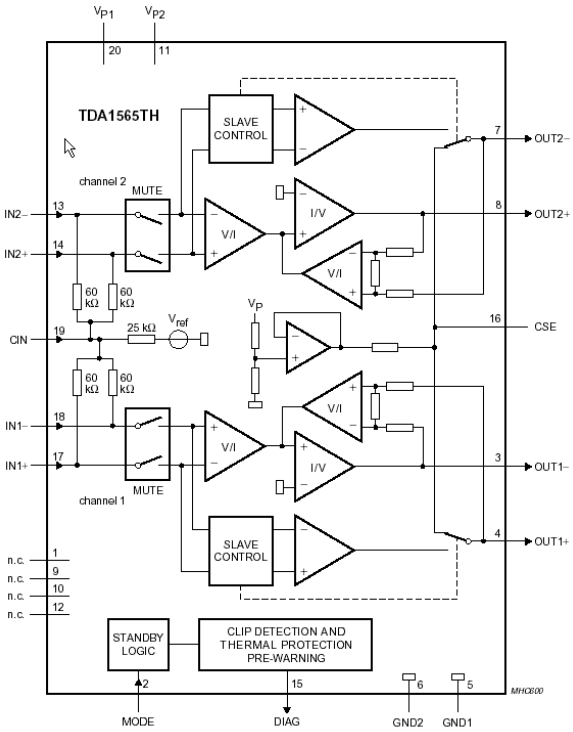
TDA1564TH



TDA1564J



TDA1565



1.3 Pinning

TDA1564

PINNING

SYMBOL	PIN		DESCRIPTION
	TDA1564TH	TDA1564J	
n.c.	1	–	not connected
MODE	2	6	mute/standby/operating
OUT1–	3	7	inverting output 1
OUT1+	4	8	non-inverting output 1
GND1	5	9	ground 1 (ground, J version)
GND2	6	–	ground 2
OUT2–	7	10	inverting output 2
OUT2+	8	11	non-inverting output 2
OC2	9	12	offset capacitor 2
n.c.	10	–	not connected
V_{P2}	11	13	supply voltage 2
OC1	12	14	offset capacitor 1
IN2–	13	16	inverting input 2
IN2+	14	17	non-inverting input 2
DIAG	15	15	diagnostic
CSE	16	4	electrolytic capacitor for single-ended (SE) mode
IN1+	17	1	non-inverting input 1
IN1–	18	2	inverting input 1
CIN	19	3	common input
V_{P1}	20	5	supply voltage 1

TDA1565

PINNING

SYMBOL	PIN	DESCRIPTION
n.c.	1	not connected
MODE	2	mute/standby/operating mode selection
OUT1–	3	inverting channel 1 output
OUT1+	4	non-inverting channel 1 output
GND1	5	ground 1
GND2	6	ground 2
OUT2–	7	inverting channel 2 output
OUT2+	8	non-inverting channel 2 output
n.c.	9	not connected
n.c.	10	not connected
V_{P2}	11	supply voltage 2
n.c.	12	not connected
IN2–	13	inverting channel 2 input
IN2+	14	non-inverting channel 2 input
DIAG	15	diagnostic output
CSE	16	electrolytic capacitor for SE mode
IN1+	17	non-inverting channel 1 input
IN1–	18	inverting channel 1 input
CIN	19	common input
V_{P1}	20	supply voltage 1

1.4 Quick Reference Data

TDA1564

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage	DC biased	6.0	14.4	18	V
		non-operating	–	–	30	V
		load dump	–	–	45	V
I_{ORM}	repetitive peak output current		–	–	4	A
$I_{q(tot)}$	total quiescent current	$R_L = \infty$	–	95	150	mA
I_{stb}	standby current		–	1	50	μA
$\|Z_i\|$	input impedance		90	120	150	kΩ
P_o	output power	R_L = 4 Ω; EIAJ	–	38	–	W
		R_L = 4 Ω; THD = 10%	23	25	–	W
		R_L = 4 Ω; THD = 2.5%	18	20	–	W
G_v	voltage gain	P_o = 1 W	25	26	27	dB
CMRR	common mode rejection ratio	f = 1 kHz; R_s = 0 Ω	–	80	–	dB
SVRR	supply voltage ripple rejection	f = 1 kHz; R_s = 0 Ω	45	65	–	dB
$\|\Delta V_O\|$	DC output offset voltage		–	–	100	mV
α_{cs}	channel separation	R_s = 0 Ω; P_o = 15 W	40	70	–	dB
$\|\Delta G_v\|$	channel unbalance		–	–	1	dB

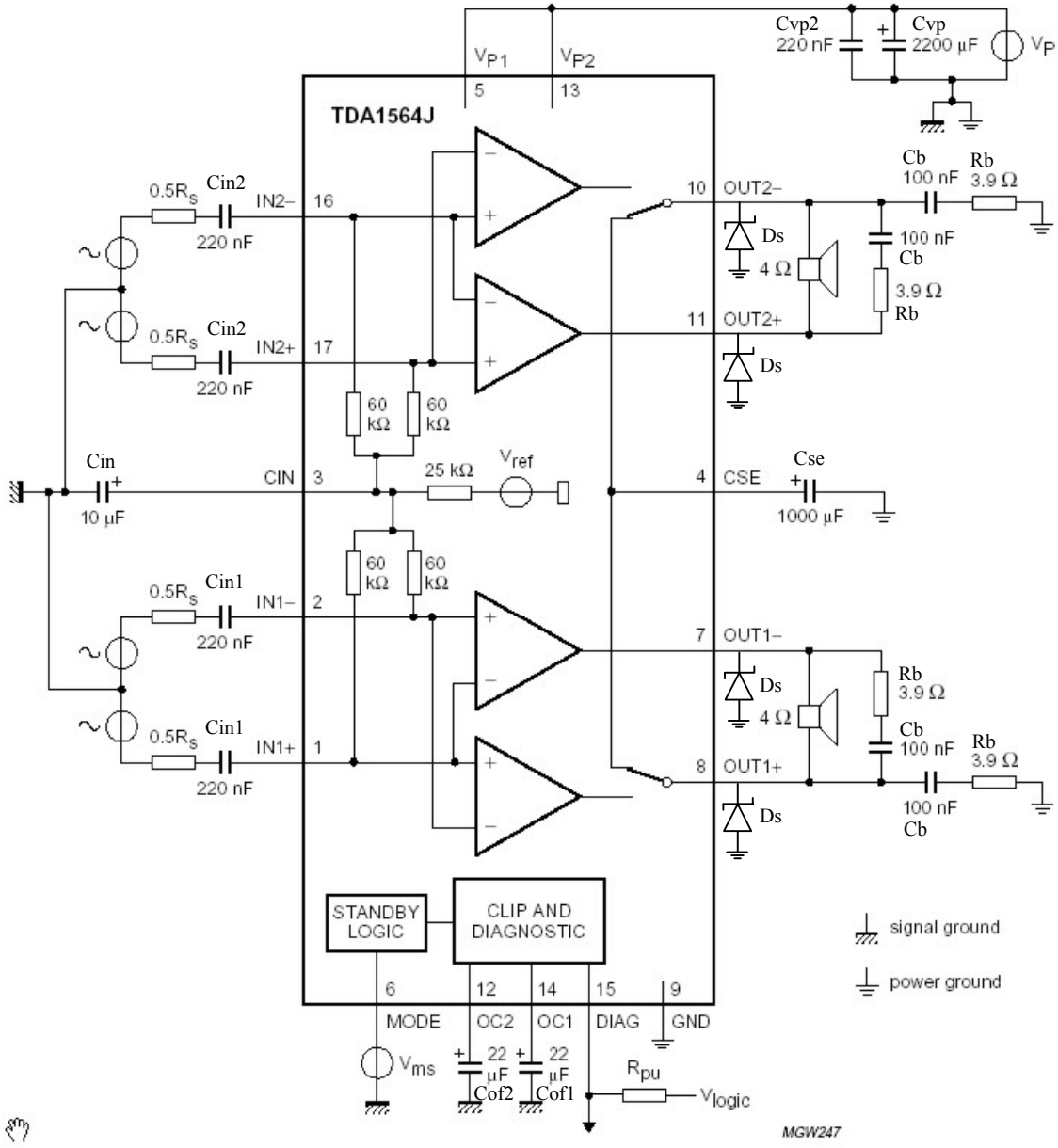
TDA1565

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage	DC-biased	6.0	14.4	18	V
		non-operating	–	–	30	V
		load dump	–	–	45	V
I_{ORM}	repetitive peak output current		–	–	8	A
$I_{q(tot)}$	total quiescent current	$R_L = \infty$	–	95	150	mA
I_{stb}	standby current		–	1	50	μA
$\|Z_i\|$	differential input impedance		90	120	150	kΩ
P_o	output power	R_L = 2 Ω; THD 0.5 %	25	31	–	W
		R_L = 2 Ω; THD 10 %	37	40	–	W
		R_L = 2 Ω; EIAJ	–	60	–	W
G_v	voltage gain		25	26	27	dB
CMRR	common mode rejection ratio	f = 1 kHz; R_s = 0 Ω	–	80	–	dB
SVRR	supply voltage ripple rejection	f = 1 kHz; R_s = 0 Ω	50	65	–	dB
$\|\Delta V_O\|$	DC output offset voltage		–	–	100	mV
α_{cs}	channel separation	R_s = 0 Ω; P_o = 25 W	50	70	–	dB
$\|\Delta G_v\|$	channel unbalance		–	–	1	dB

2. APPLICATION DESCRIPTION

2.1 Application Diagram TDA1564

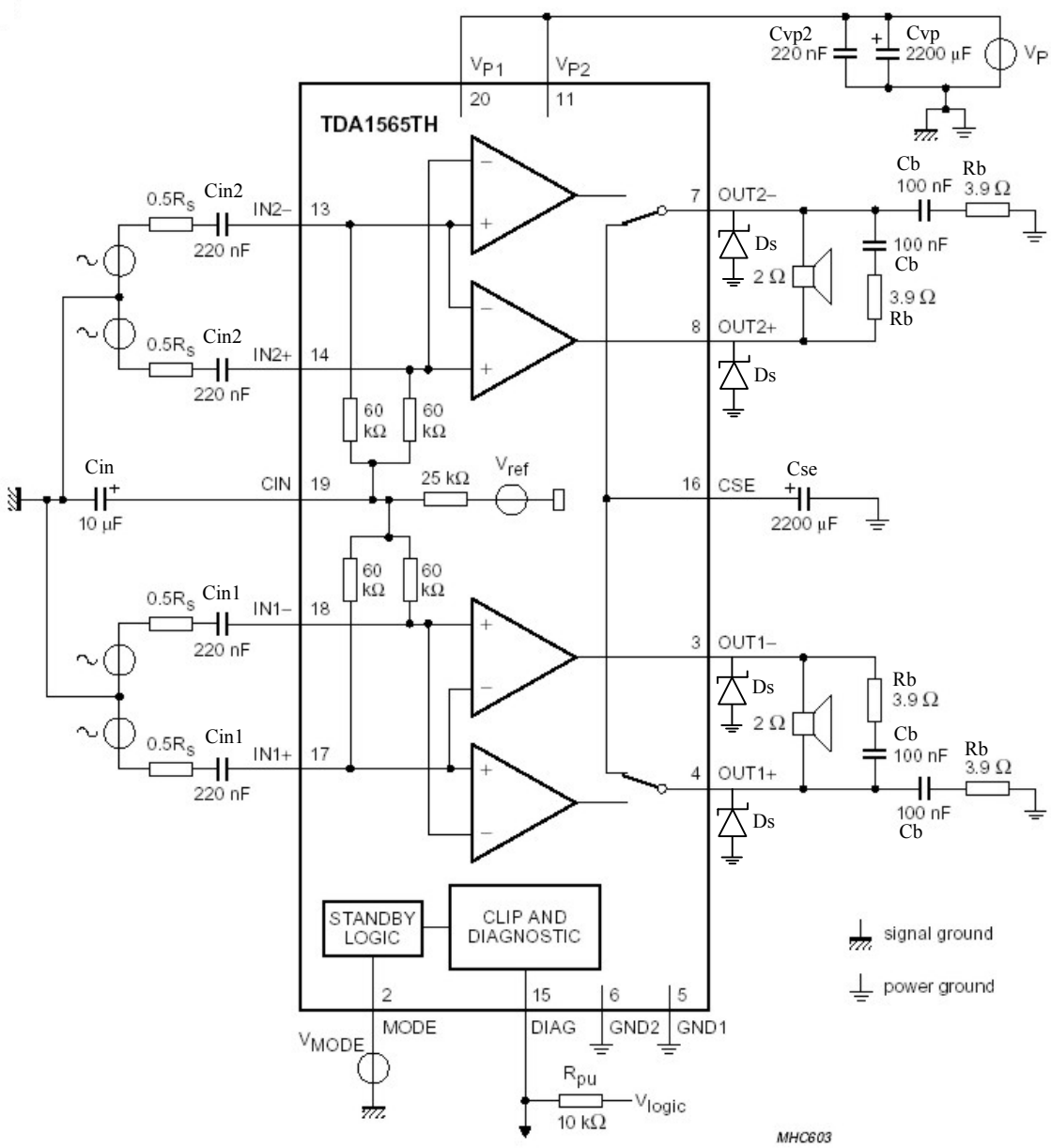


The following remarks about the application diagram can be given :

- In order to get a proper stability, the boucherot filters at the outputs should be connected as close as possible to the pins of the device
- The capacitors on the OC1 and OC2 pins are intended for filtering the internal signal for the DC offset detection at the outputs. In this way the offset detection comparators are not unnecessary enabled during regular AC music signals which are larger than 2V

- The SE capacitor at the CSE output should be 1000uF, in order to minimize the dissipation at low frequencies, in SE mode
- The capacitor of 10uF at the CIN pin is to reject the supply voltage ripple of the internal reference voltage of the input stage
- The input capacitors are for a DC coupling and have a low frequency roll-off function
- The DIAG pin is an open collector output, so a pull-up resistor is necessary to monitor the diagnostics. During a fault condition the signal is active low
- In order to get a proper protection against a loss of ground condition, a schottky diode at each output to ground is recommended (see paragraph "protections")

2.2 Application Diagram TDA1565



The following remarks about the application diagram can be given :

- In order to get a proper stability, the boucherot filters at the outputs should be connected as close as possible to the pins of the device
- The SE capacitor at the CSE output should be 2200uF (higher than the capacitor value of the TDA1564, due to the higher output power) in order to minimize the dissipation at low frequencies, in SE mode

- The capacitor of 10uF at the CIN pin is to reject the supply voltage ripple of the internal reference voltage of the input stage. The input capacitors are for DC coupling and a low frequency roll-off (increasing CIN means a lower frequency roll-off and vice versa)
- The DIAG pin is an open collector output, so a pull-up resistor is necessary to monitor the diagnostics. During a fault condition the signal is active low
- In order to get a proper protection against a loss of ground condition, a schottky diode between each output and ground is recommended (see paragraph "protections")

2.3 Used Components

Component	Value	Comment	Purpose
Cin	10uF/16V	Elco	Reference voltage ripple rejection capacitor
Cin1, Cin2	220nF	MKT	Input DC coupling
Cvp	2200uF/16V	Elco	Buffer capacitor
Cvp2 *	220nF	MKT	HF decoupling
Cof1, Cof2 **	10uF/16V	Elco	DC offset detection filter capacitor
Cse	1000uF/16V *** 2200uF/16V ****	Elco	Single Ended capacitor
Cb	100nF	SMD npo	Boucherot with Rb
Rb	3.9 Ohm	SMD 1/4W	Boucherot with Cb
Rpu	10k	SMD	Pull up resistor for diagnostics
Ds	BAT140A or BYV10-40	SMD (double schottky in SOT223) SOD81	Schottky diode for loss of ground protection

* see "pcb layout recommendations" for explanation

** only for TDA1564

*** for TDA1564

**** for TDA1565

2.4 Protections

2.4.1 Loss of ground

The definition of a loss of ground with a power amplifier can be described as following :

The ground of the power supply (car-battery) is connected to the output of the amplifier, instead of to the amplifier-ground, after which the amplifier is turned-on.

In a practical situation a loss of ground condition could occur during assembly in the factory, the car manufacturer (OEM) or in the case of an aftersales customer.

In order to protect the amplifier in such a condition, it is recommended to use a schottky diode between each of the amplifier outputs and ground, as close as possible to the pins of the device. Refer to the application diagram.

The recommended schottky diodes are one of the following :

Philips BVY10-40 or an SMD type; Philips BAT140A , two schottky's in one SMD housing, for a space saving PCB mounting.

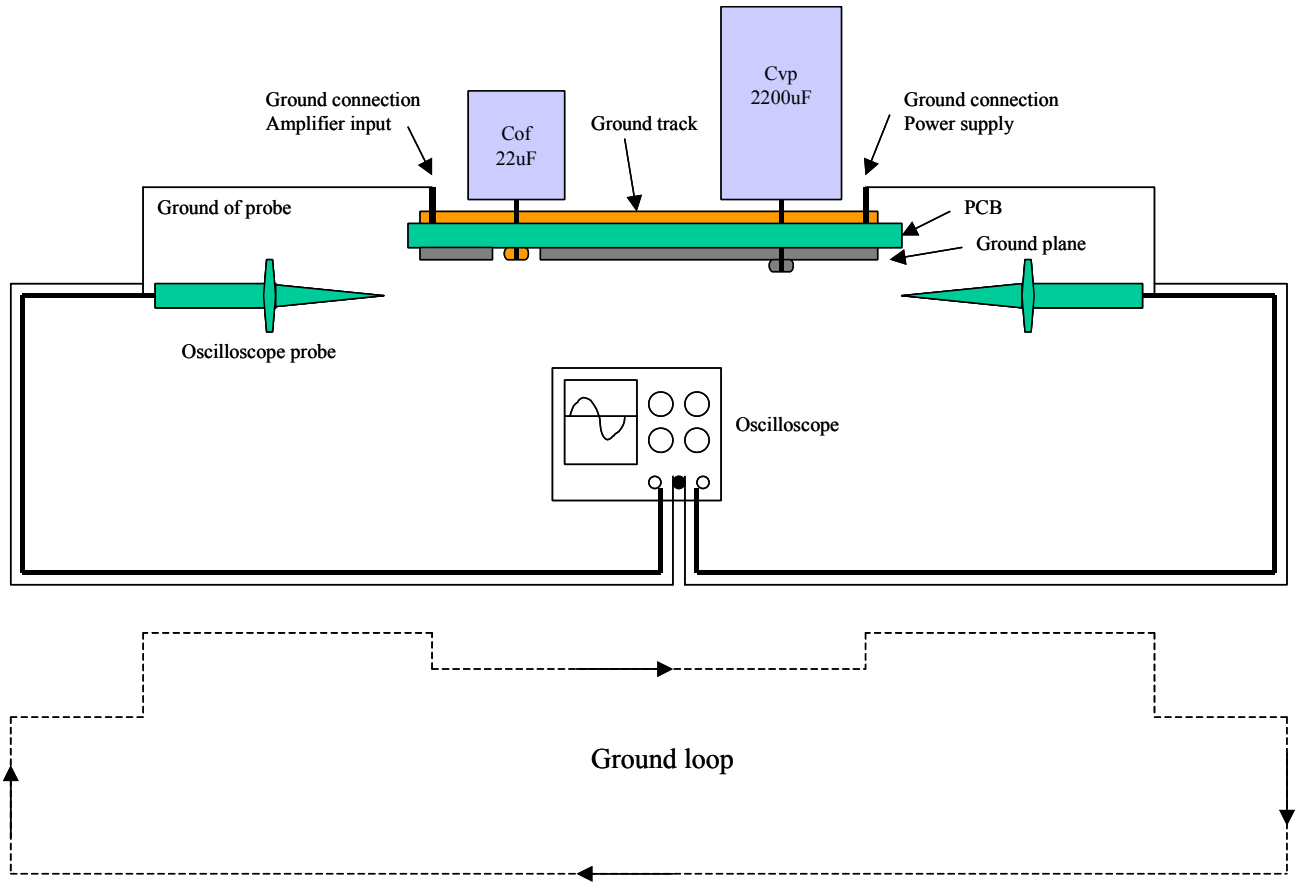
2.5 Critical Conditions

2.5.1 Ground loops

Ground loops are unwanted signal paths that can occur during measurements of the power amplifier, which can result in a higher THD performance of the amplifier. A many seen fault is after connecting two ground connectors of an oscilloscope probe : one at the signal ground of the input of the amplifier and one on the ground of the power supply.

The same condition holds when connecting an audio analyser (Audio Precision). In this case when the ground connector (cable shield) is connected to the amplifier input signal ground and when the output is measured, while its ground connector (cable shield) is connected to the power supply ground.

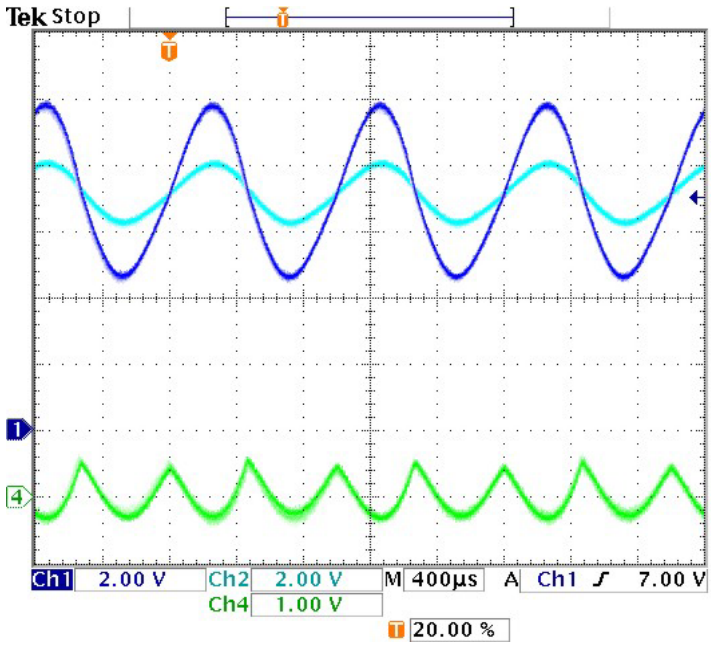
The following drawing shows such a ground loop condition.



In practice one should always try various ground connections when measuring THD. However, in many cases it is adviced to use only one ground connection from the measuring device to the power amplifier board.

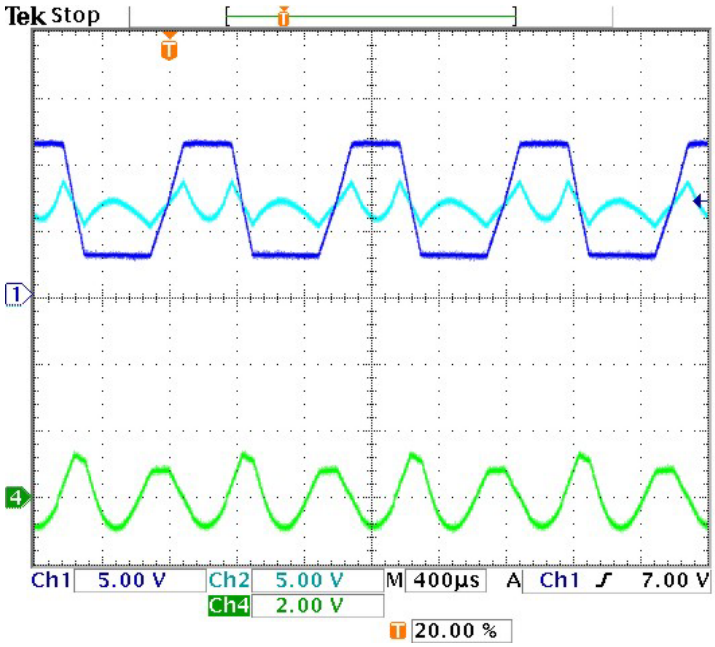
To check if a ground loop is present, measure the distortion residue on an oscilloscope together with the output signals of the amplifier. The distortion residue is usually a monitor output on an audio analyser, eg. Audio Precision System Two, which shows the difference between the shape of the original waveform that is put on the input of the power amplifier and the waveform that is present on the output. (be aware of that System Two does not scale this distortion residue !)

The distortion residue shows a groundloop; the waveform shows **the rectified frequency** of the signal that is put on the amplifier inputs. The following pictures show two examples of a ground loop.



Ground loop during low output power

The green line represents the distortion residue (not scaled!) at which the rectified frequency can be recognized. The blue and cyan lines represent the amplifier outputs which are explained in the paragraph "Typical Waveforms".



Ground loop during high output power

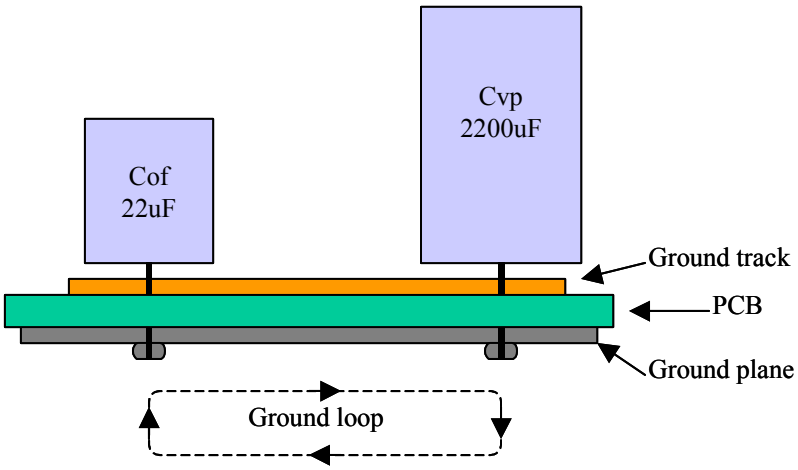
As can be seen is that the distortion residue can change from shape due to the high output power.

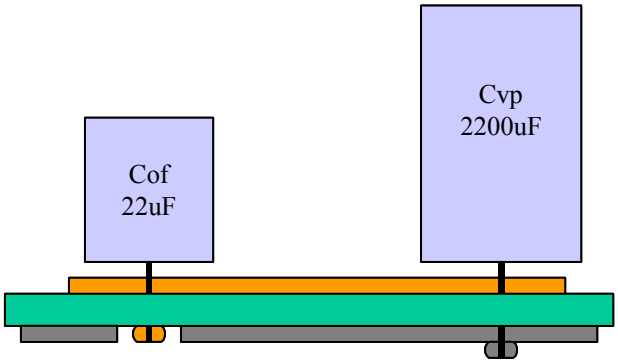
Furthermore, in general a ground loop can be recognized by an increase in the THD=f(frequency) curve.

2.6 PCB Layout recommendations

The following recommendations can be given when designing a PCB

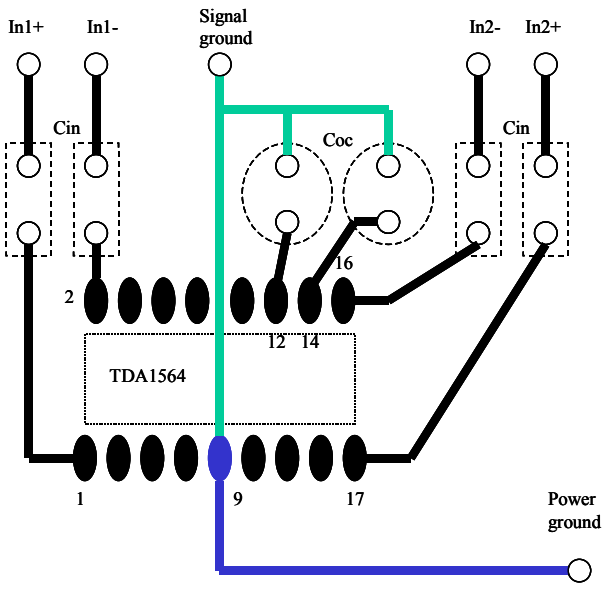
- Don't situate input tracks nearby output tracks to prevent interference
- (*) Use a HF decoupling capacitor of about 220nF nearby the device, between each Vp and power ground connection
- When for the Boucherot filters or for the HF decoupling capacitors on Vp, SMD components are used, be aware of differences in behaviour w.r.t. the capacitor material. Good results are found with NPO capacitors which have a low ESR, next are X7R capacitors and last are Y5V capacitors which have a considerable ESR
- Place the Boucherot filters as close as possible to the amplifier output pins
- In order to minimize the losses in the tracks for Vp and power ground during high output power, use 75um or thicker copper layer and use a track-width of at least 5mm
- When using a ground plane, prevent ground loops which have a negative effect on the THD performance. Use only one connection from the ground plane to ground, eg at the buffer capacitor of Vp. The following drawing shows an example of a proper grounding and a poor grounding



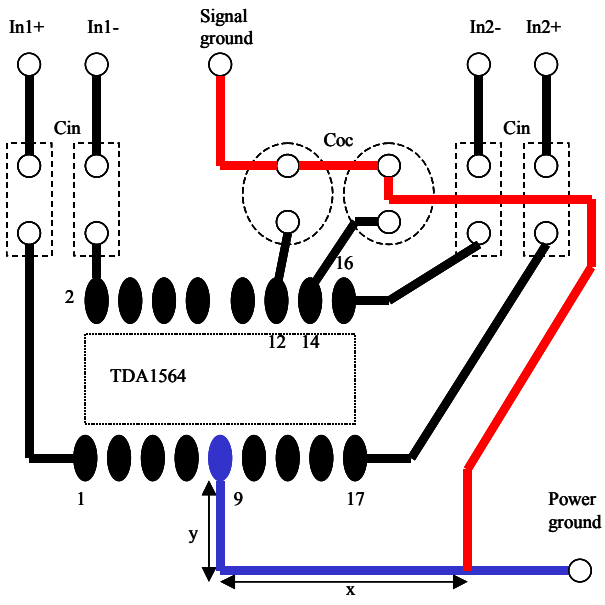


No Ground loop

- In spite of the fact that this amplifier has differential inputs, which performs a lot better on ground noise than an amplifier with unbalanced inputs, separate the small signal ground connection from the power ground connection that leads to the power supply (car battery), to prevent possible interference of any disturbances that come from the power supply
- The ground references of the amplifier should all have the same potential. This is to prevent dc shifts between the different grounds. In practice this can be done by choosing a star ground connection between power ground and signal ground (DC voltage shifts could otherwise occur through the large currents that flow through the power ground tracks) The next drawing shows an example between a proper lay-out and a poor one



Good



Not Good

As can be seen in the left picture is that the signal ground potential of the ground pin (9) is equal to the potential of the minus pole of the Coc (offset) capacitors and the signal ground connector of the input signal.

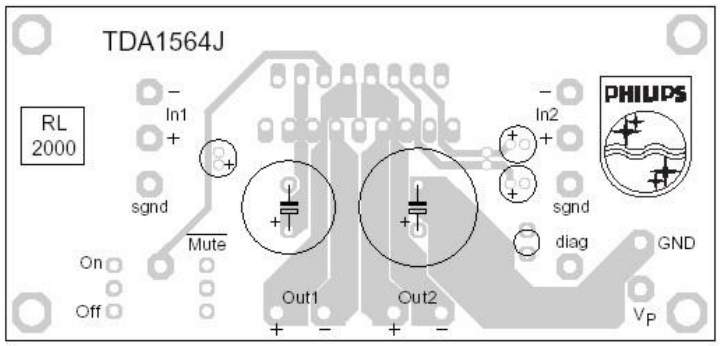
In the right picture the potential between pin 9 and the signal ground connector is unequal, depending on the current-flow through the track, x+y.

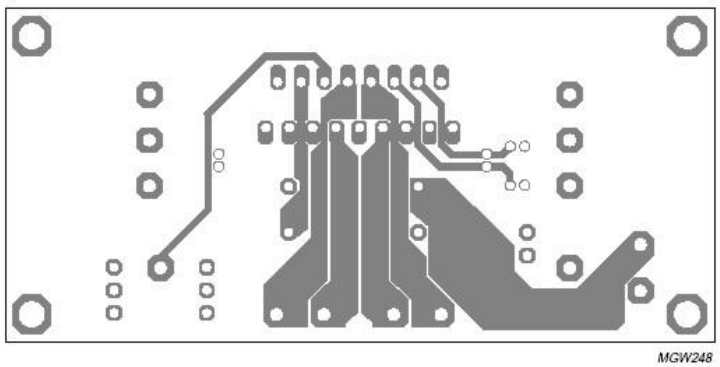
Suppose that, at a certain output power, the current through the x+y ground track equals 3A , while the resistance of the track x+y equals 100mOhm, then the voltage across x+y equals 0.3V and will increase with increasing output power.

2.7 PCB Layout demoboard

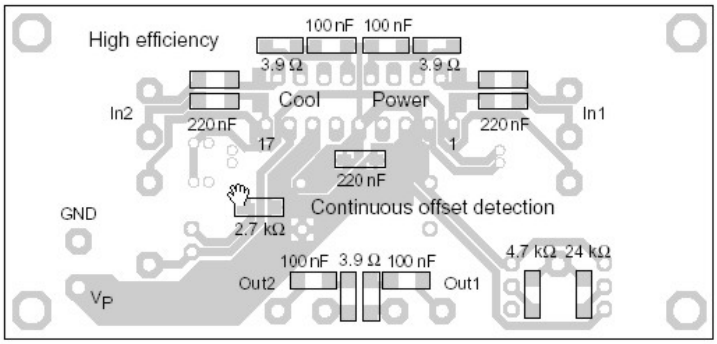
2.7.1 TDA1564J

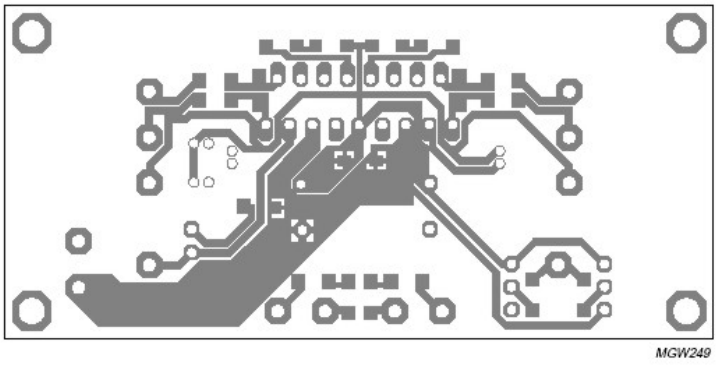
The following pictures show the pcb layout of a demoboard for the TDA1564J with a DBS17P package.





top view

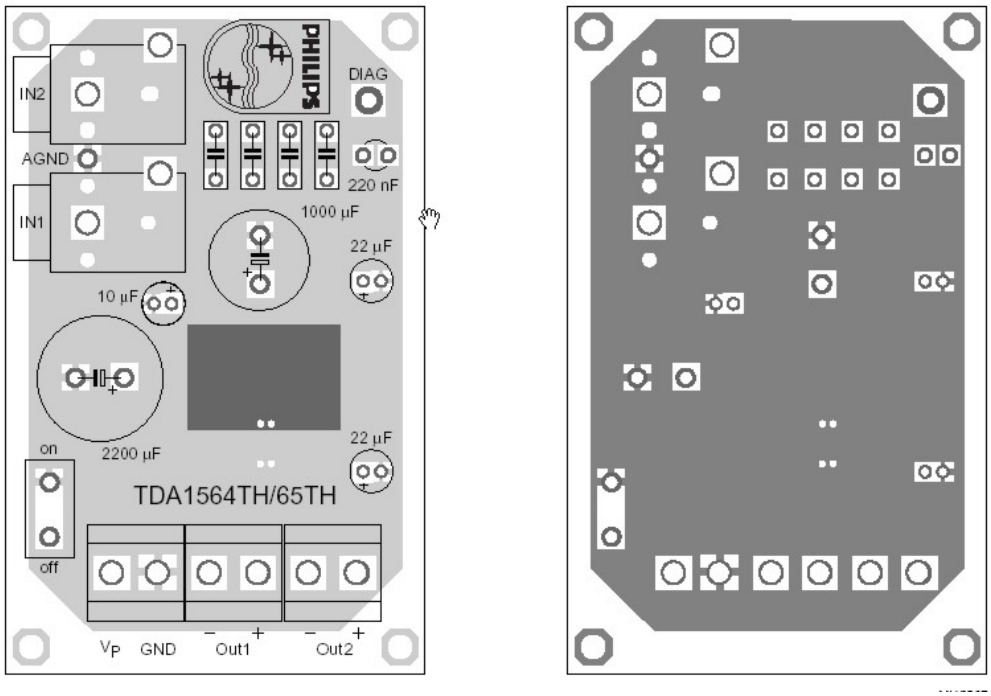

High efficiency
100 nF 100 nF
3.9 Ω
3.9 Ω
In2
Cool
Power
In1
220 nF
220 nF
17
1
220 nF
GND
Continuous offset detection
2.7 kΩ
4.7 kΩ 24 kΩ
100 nF 3.9 Ω 100 nF
Out2
Out1
VP


MGW249

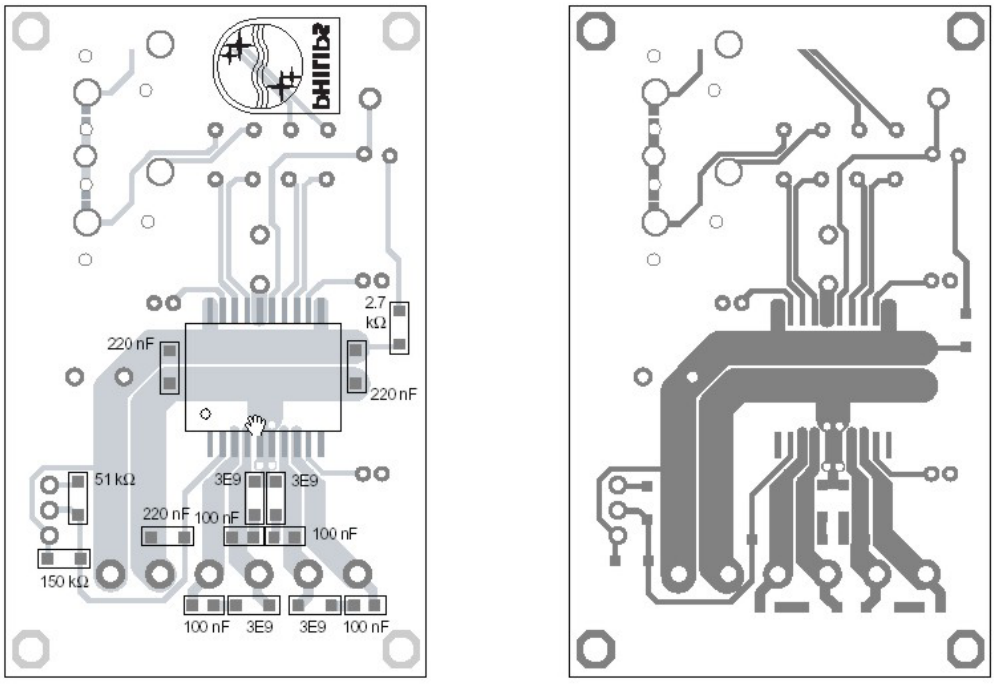
Bottom view

2.7.2 TDA1565TH

The following pictures show the pcb layout of a demoboard for the TDA1564 and a TDA1565 with a HSOP20 package.



Top view



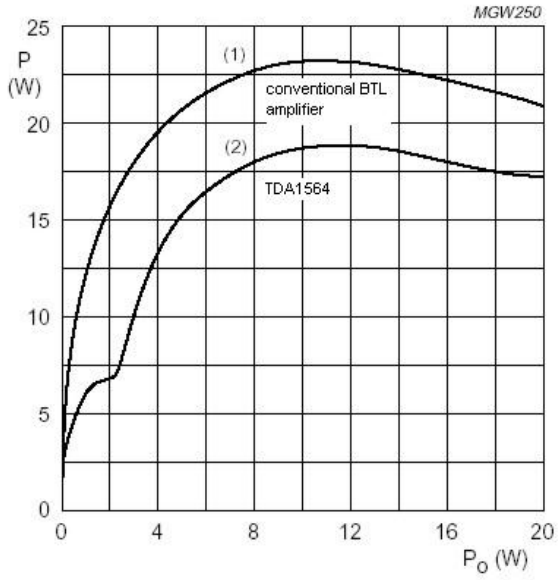
Bottom view

2.8 Heatsink calculation

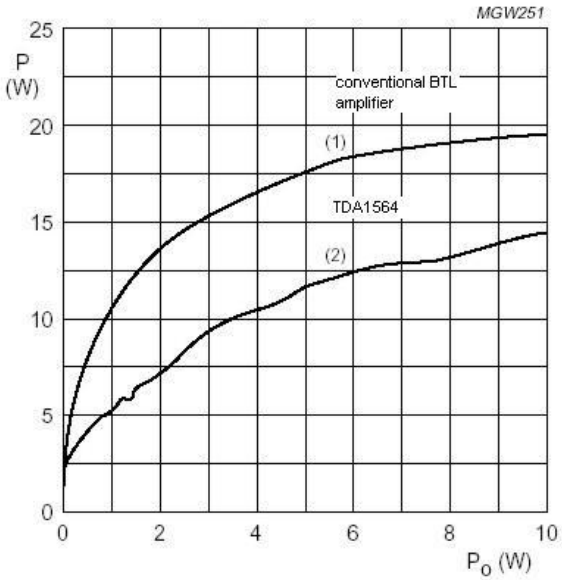
An appropriate heatsink can be calculated by using one of the next figures that show the curve of the power dissipation as function of the output power of one channel. The left pictures are valid for a sinewave signal of 1kHz, while the right ones are for pink noise through a IEC-60268 filter (-3dB Bandwidth : 60Hz … 3kHz).

Pink noise through an IEC-60268 filter represents an average music signal.

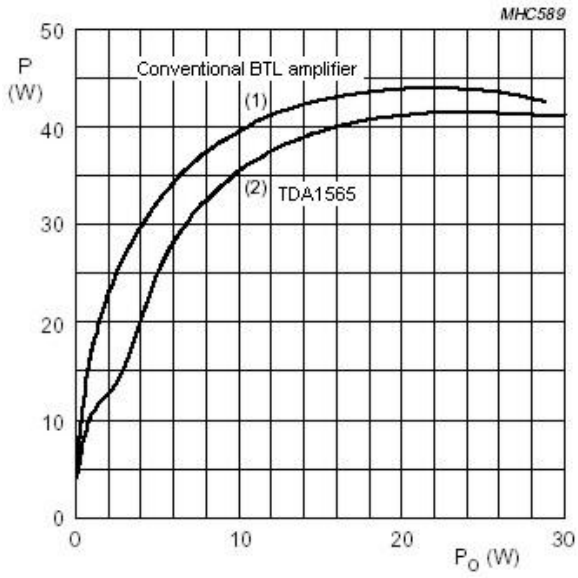
Curve (1) is for a conventional BTL amplifier and should not be used for this calculation, it only shows the difference in dissipation between BTL and this high efficiency amplifier.



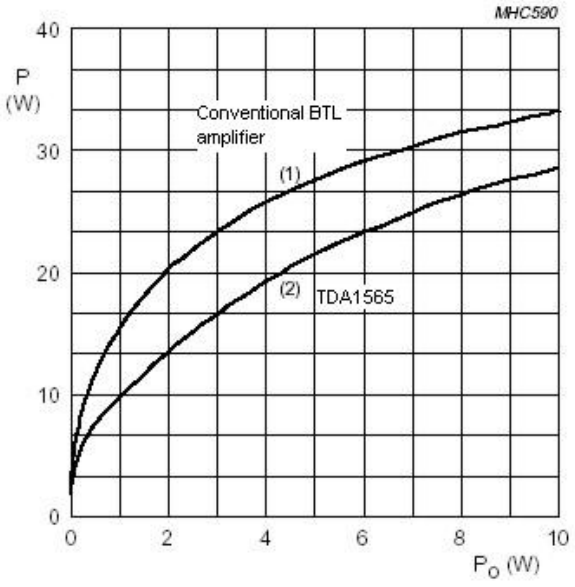
TDA1564 1kHz sinewave 4 Ohm



TDA1564 pink noise , IEC-60268 4 Ohm



TDA1565 1kHz sinewave 2 Ohm



TDA1565 pink noise , IEC-60268 2 Ohm

The calculation is as following :

1. Choose the amount of output power on the X-axis and draw a straight vertical line through the curve of the dissipation
2. Read off the value on the Y-axis which meets the crossing point of the vertical line and the dissipation curve
3. Fill in this value in the formula (1) when the amplifier is used in mono applications or
4. Double it and fill in this value in the formula (1), just as the other known values

eg. if the TDA 1564 should deliver a stereo music output power of 2 x 1 W into 4 Ohm, in an ambient temperature of 65 Degrees Celsius, without going into temperature protection, then the thermal resistance of the heatsink is calculated as following :

The total output power equals :

$P_{out\_music} = 2x1W$, on the X-axis in the figure this means 1W !

Read out the power dissipation :

$P_{diss} = 5W$, for a stereo application this becomes $P_{diss\_tot} = 10W$

The ambient temperature equals :

$T_{amb} = 65°C$

The temperature pre-warning according the specification equals :

$T_{pre} = 145°C$

The thermal resistance of the HSOP20 package according to the specification equals :

$R_{th(vj-c)} = 1.3K/W$

When using thermal paste between the package and the heatsink then :

$R_{th(c-h)} = 0.1K/W$

The thermal resistance of the heatsink can then be calculated :

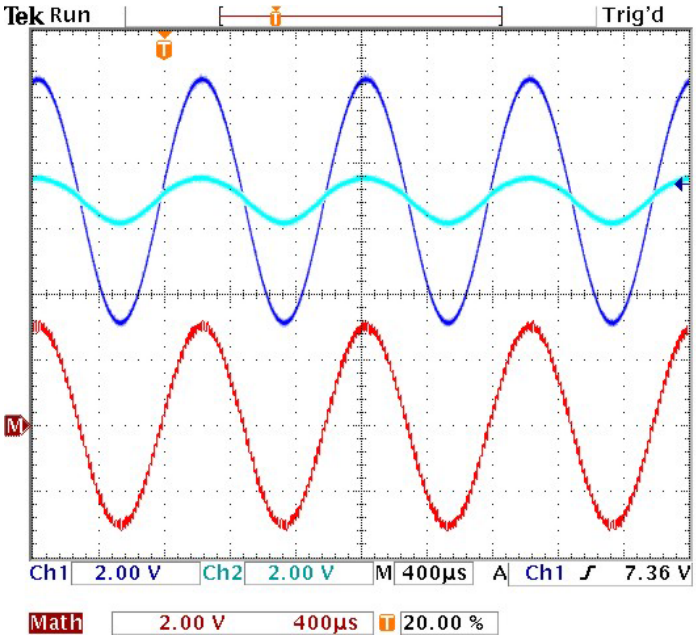
(1) $$R_{th(h-a)} = \left(\frac{T_{pre} - T_{amb}}{P_{diss\_tot}}\right) - R_{th(vj-c)} - R_{th(c-h)} = \left(\frac{145-65}{10}\right) - 1.3 - 0.1 = 6.6K/W$$

For a conventional BTL amplifier this would be 2.6K/W (!).

3. TYPICAL WAVEFORMS

The TDA1564/5 with its Cool Power feature has some unusual and unkown waveforms on the outputs of the amplifier when they are monitored with an oscilloscope. In order to get acquainted with these waveforms, this paragraph shows some of those typical waveforms during various conditions.

- Single ended mode , Vload < 2.5Vrms at 4 Ohm load and Vp=14.4V

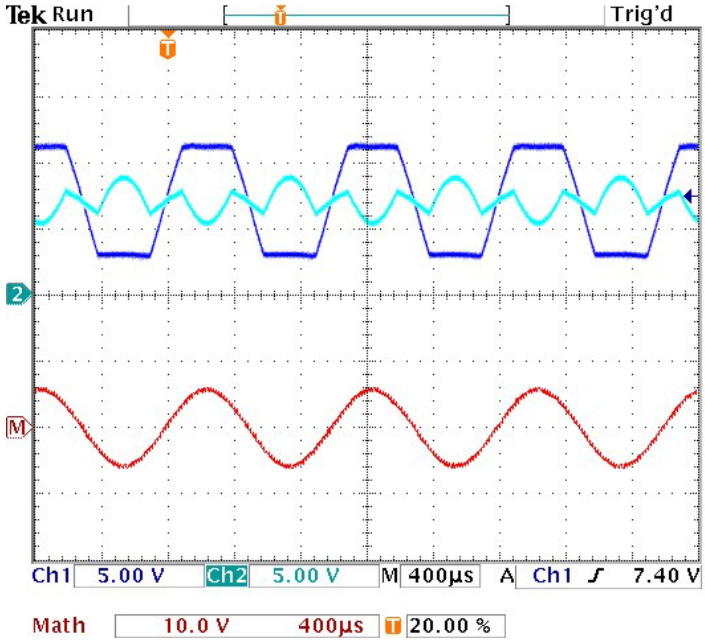


As can be seen is that the slave output voltage (cyan line) is in phase with the master output voltage (blue line), so the amplifier is still in single ended mode which results in the voltage across the load (red line).

The signal across the load equals $V_{load} = V_{master} - V_{slave}$

(the signal across the load is somewhat rippled, this is due to the sample rate of the math function of the oscilloscope and is not caused by the amplifier)

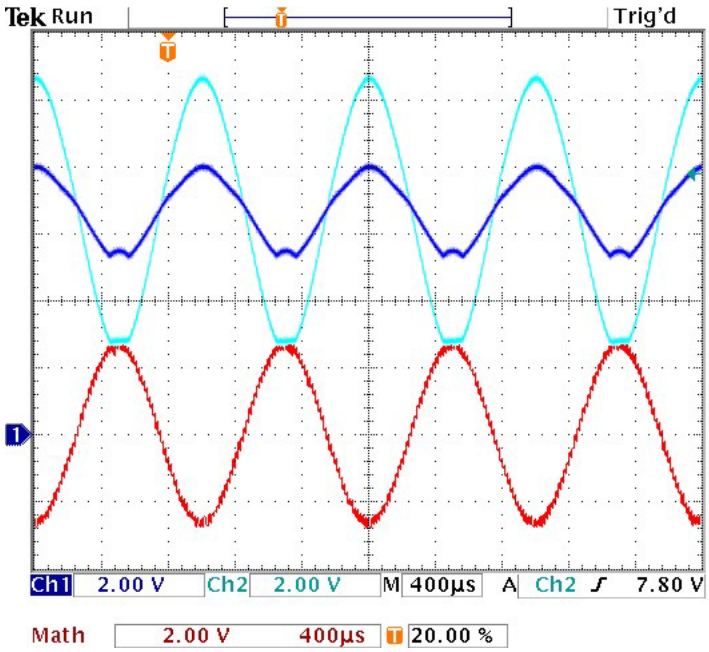
Bridge Tied Load mode, Vload >2.5Vrms at 4 Ohm load and Vp=14.4V



Now the slave output voltage (cyan line) is of opposite phase with the master output voltage (blue line), so the amplifier is in BTL mode which results in a sine wave across the load (red line).

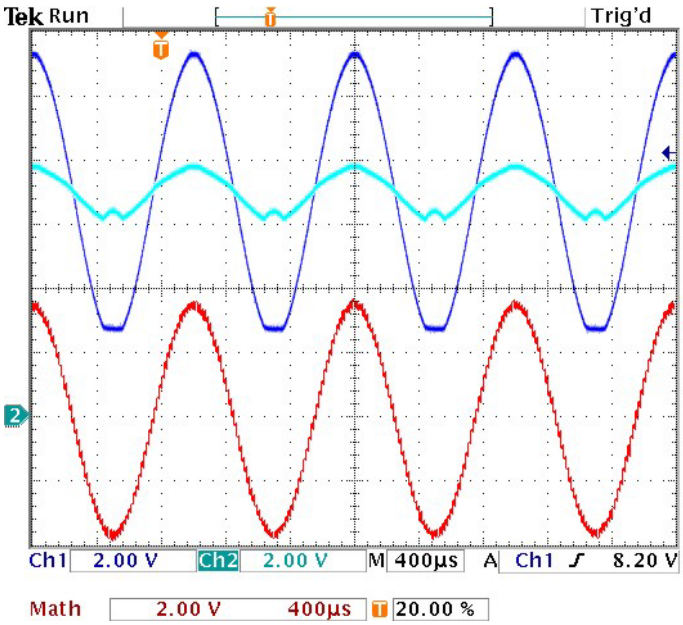
The signal across the load still equals $V_{load} = V_{master} - V_{slave}$

- Switch over point with 2 ohm load and Vp=14.4V (TDA1565 only)

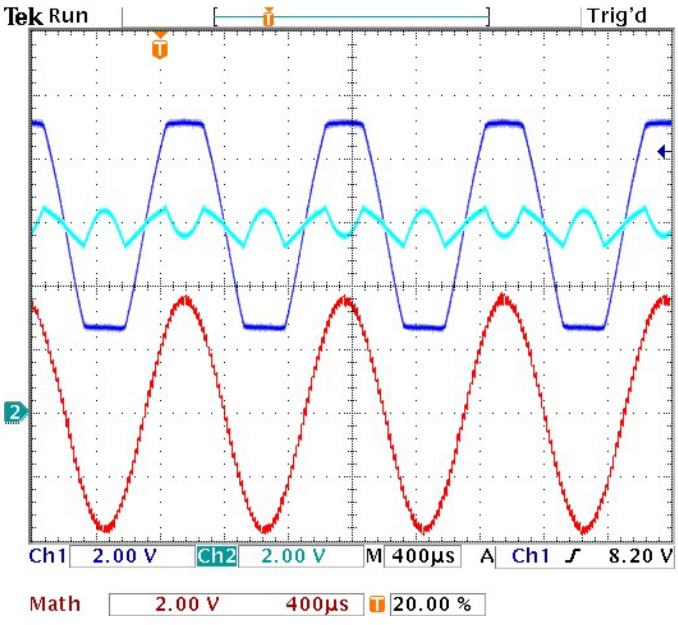


This picture is of just after switching over to BTL mode. The switch over point for a 2 Ohm load is lower since the output current is larger and so the master output has less 'room' than with a 4Ohm load. The output voltage equals about 1.7Vrms.

- Switch over point at different Vp values



This picture shows the moment just after switching to BTL, when Vp = 14.4V



This picture shows the moment just after switching to BTL, when Vp = 12V and the input signal has the same value as in the previous picture. As can be seen is that the master output (blue line) has less room (1/2 Vp = 6V) when the Vp is lowered and therefore the slave output (cyan line) must also drive the load.